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EXAMINER	
NGUYEN, LINH V	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,149	MOYAL ET AL.	
	Examiner	Art Unit	
	Linh V Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *24 February 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

1. This office action is in response to applicant's amendment received on 2/24/03. Claims 1 – 21, are pending on this application.

EXAMINER'S COMMENTS

2. Pub. No.: US2002/0153959 A1 is an English translation for DE-19946200A1.

Response to Arguments

3. Applicant's arguments with respect to amended claims 1, 15, 16, and 21 have been considered but not persuasive from the following:

On page 14 of amendment received on 2/24/03, applicant's argued that Gotz does not appear to disclose or multi-bit lock signal. Examiner respectfully traverses

Fig. 1 of Gotz et al. disclose a phase lock loop having MUX1 and MUX2 response to a lock signal output from control logic (CL) to select a reference frequency (MUX2) as said input frequency (output from FT3) and select a first feedback ratio (MUX2) when in a first mode; and select a divided frequency (output from FT4) of said input frequency as said input frequency and select a second feed back ratio, when in a second mode; wherein a first bit of said multi-bit lock signal selects said first feedback ratio and a second bit of said multi-bit lock signal selects said second feedback ratio (this is inherently to Gotz et al. because the structure suggested by Gotz et al. is similar to the present invention, then the function is intrinsic to the PLL of Gotz et al.) Although Gotz et al. is silence to the term "multi-bit" lock signal from his lock signal for MUX1 and

MUX2). However the lock signal of Gotz et al is providing the same function and concept of the multi-bit lock signal of claimed invention, therefore the term "multi-bit" must be intrinsic or inherently to the lock signal of Gotz et al. Furthermore applicant fails to point out the "multi-bit" of claimed invention is having any elements or structures which are distinct over the lock signal of Gotz et al, besides the terminology of "multi-bit".

Regarding to new claim 21, Gotz et al. as applied to claim 1, 15, and 16 above, teaching a Phase lock loop comprising every aspect of applicant claimed invention except for the lock signal of Gotz et al. is response to internal input instead of external user input of applicant's invention. However the internal input of control logic (CL) of Gotz et al. is response to the external user input TW and TWR; therefore the output lock signal from control logic (CL) is indirectly response to the external user input TW and TWR of Fig. 1.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1 – 4, 6, 9 – 12, and 14 – 21, are rejected under 35 U.S.C. 102(e) as being anticipated by Gotz et al. German patent No. 19946200 A1 (English translation US2002/0153959 A1).

Regarding to claims 1, Fig. 1 of Gotz et al. disclose a phase lock loop having MUX1 and MUX2 response to a lock signal output from control logic (CL) to select a reference frequency (MUX2) as said input frequency (output from FT3) and select a first feedback ratio (MUX2) when in a first mode; and select a divided frequency (output from FT4) of said input frequency as said input frequency and select a second feed back ratio, when in a second mode; wherein a first bit of said multi-bit lock signal selects said first feedback ratio and a second bit of said multi-bit lock signal selects said second feedback ratio (this is inherently to Gotz et al. because the structure suggested by Gotz et al. is similar to the present invention, then the function is intrinsic to the PLL of Gotz et al.) Although Gotz et al. is silence to the term "multi-bit" lock signal from his lock signal for MUX1 and MUX2). However the lock signal of Gotz et al is providing the same function and concept of the multi-bit lock signal of claimed invention, therefore the term "multi-bit" must be intrinsic or inherently to the lock signal of Gotz et al. Furthermore applicant fails to point out the "multi-bit" of claimed invention is having any elements or structures which are distinct over the lock signal of Gotz et al, besides the terminology of "multi-bit".

Regarding to claim 2, wherein the first mode is further configured to increase a feedback divide ratio (f2MUX1).

Regarding to claim 3, wherein the second mode is further configured to decrease the feedback divide ratio (f1MUX1).

Regarding to claim 4, wherein the lock circuit comprises a lock decision logic circuit (CL).

Regarding to claim 6, wherein the lock circuit is configured in response to an internal signal (output signal of change over control circuit (US)).

Regarding to claim 9, wherein the PLL comprises: a first switchable divider (MUX2) configured to generate a reference frequency in response to the input frequency; a PLL logic circuit configured to generate the output frequency (fVCO) in response to the reference; and a second switchable divider (MUX1) configured to generate feedback frequency in response to said output frequency.

Regarding to claim 10, wherein said first and second switchable dividers are further configured in response to said lock signal (see Fig. 1).

Regarding to claim 11 wherein the first switchable divider comprises a first divider (FT4) and a first multiplexer (MUX2), wherein the first multiplexer is configured to select the first divided output frequency or the input frequency and present the reference frequency; and the second switchable divider comprises a second divider (FT1), a third divider (FT2) and a second multiplexer (MUX1), wherein said multiplexer is configured to select a second divided output frequency or a third divided frequency and present the feedback frequency (f1MUX1, f2MUX1).

Regarding to claim 12, wherein said second and third dividers are configured in series (FT1, FT2).

Regarding to claim 14, where in second and third dividers comprise multi-channel dividers (page 2 lines 4 –6, disclosing PLL circuit for TDMA, GSM systems, therefore multi-channel is inherent to PLL circuit of Gotz et al.).

Regarding to claim 15, Fig. 1 Gotz et al. disclosing circuit having: means for multiplying an input frequency in response to a lock signal; means for generating an output frequency in response to said input frequency; means for generating said lock signal; means for selecting said input frequency to be a reference frequency when in a first mode and a divided frequency of said input frequency when in a second mode.

Regarding to claims 16 – 20, the steps in the claimed method are deemed to be made clearly taught by Gotz et al. as applied to claims 1 – 4, 9 – 12, and 15 above.

Regarding to new claim 21, Gotz et al. as applied to claim 1, 15, and 16 above, teaching a Phase lock loop comprising every aspect of applicant claimed invention except for the lock signal of Gotz et al. is response to internal input instead of external user input of applicant's invention. However the internal input of control logic (CL) of Gotz et al. is response to the external user input TW and TWR; therefore the output lock signal from control logic (CL) is indirectly response to the external user input TW and TWR of Fig. 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gotz et al.

Gotz et al. as applied to claim 11 above disclose every aspect of applicant's claimed invention except that wherein said second and third dividers are configured in parallel. Fig. 1 Gotz et al. shows dividers (FT, FT2) circuit arrangement is an equivalent structure know in the art and furthermore this equivalent circuit also has indicated by applicant with respect to Fig. 5, 6 or Fig. 7, 8 of applicant application. Therefore Gotz et al. structures are equivalent to applicant's claimed invention.

8. Claims 5, 7 and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Gotz et al. in view of Lada, Jr. et al. U.S patent No. 5, 142, 247.

Gotz et al. as applied to claim 1 above disclose every aspect of applicant's claimed invention except wherein the control logic circuit comprises a timer, and a user externally controls the lock circuit.

Fig. 2 Lada discloses a Phase Lock Loop circuit having a lock logic circuit (30) externally controlled by a user (SEL) to generate a lock signal (REFSEL) wherein the lock logic circuit is extern comprises a timer (33).

Gotz et al. and Lada, Jr. et al., are analogous because they are from similar problem solving for Phase Lock Loop circuit. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to apply external control of lock logic circuit with timer of Lada et al. to the internal control of lock logic

circuit of Gotz et al. for the purpose of maintaining the pulse for a predetermined number of cycles so that the pulse duration exceeds the time necessary for Phase Lock Loop to acquire and lock onto the new frequency (Lada, Col. 6 lines 41 – 47).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

April 28, 2003

Michael J. Tokar

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